

IN THE CLAIMS:

Claims 1-24 have been amended herein. All of the pending claims 1 through 24 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A semiconductor die, comprising:  
a semiconductor substrate having a front side and a back side;  
an integrated circuit on a portion of ~~said~~ the front side;  
a passivation layer covering a portion of ~~said~~ the integrated circuit causing a stress on at least a portion of the semiconductor substrate; and  
a stress-balancing layer covering at least a portion of ~~said~~ the back side substantially balancing the stress caused by the ~~front-side~~ passivation layer covering a portion of ~~said~~ the integrated circuit.
2. (Currently Amended) ~~A~~The semiconductor die in accordance with claim 1, wherein ~~said~~ the stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.
3. (Currently Amended) ~~A~~The semiconductor die in accordance with claim 1, wherein ~~said~~ the stress-balancing layer comprises an adhesive material.
4. (Currently Amended) ~~A~~The semiconductor die in accordance with claim 1, wherein ~~said~~ the stress-balancing layer comprises a layer for laser-marking.
5. (Currently Amended) ~~A~~The semiconductor die in accordance with claim 1, further comprising an adhesive layer attached to ~~said~~ the stress-balancing layer.

6. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 5, wherein ~~said the~~ adhesive layer comprises a layer of material for laser-marking.

7. (Currently Amended) A nonwarp semiconductor die, comprising:  
a semiconductor substrate having a front side, a back side, and a low ratio of height to a horizontal dimension;  
an integrated circuit on ~~said the~~ front side;  
a passivation layer covering a portion of ~~said the~~ integrated circuit exerting a stress on ~~said the~~ substrate front side; and  
a stress-balancing layer covering at least a portion of ~~said the~~ back side, ~~said the~~ stress-balancing layer for balancing a portion of ~~said the~~ front side stress with a generally equivalent back side stress.

8. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 7, wherein ~~said the~~ stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

9. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 7, wherein ~~said the~~ stress-balancing layer comprises an adhesive material.

10. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 9, wherein ~~said the~~ stress-balancing layer comprises a layer of material for laser-marking.

11. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 7, further comprising an adhesive layer attached to ~~said the~~ stress-balancing layer.

12. (Currently Amended) ~~A~~The nonwarp semiconductor die in accordance with claim 11, wherein ~~said the~~ adhesive layer ~~for laser-marking~~ comprises a layer of material for laser-marking.

13. (Currently Amended) A semiconductor die, comprising:  
a semiconductor substrate having a front side having an integrated circuit on a portion thereof and a back side;  
a passivation layer covering a portion of ~~said the~~ integrated circuit causing a stress on at least a portion of the semiconductor substrate; and  
a stress-balancing layer covering at least a portion of ~~said the~~ back side substantially balancing the stress caused by the ~~front-side~~ passivation layer covering a portion of ~~said the~~ integrated circuit.

14. (Currently Amended) The semiconductor die of claim 13, wherein ~~said the~~ stress-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

15. (Currently Amended) The semiconductor die of claim 13, wherein ~~said the~~ stress-balancing layer comprises an adhesive material.

16. (Currently Amended) The semiconductor die of claim 13, wherein ~~said the~~ stress-balancing layer comprises a layer for laser-marking.

17. (Currently Amended) The semiconductor die of claim 13, further comprising an adhesive layer attached to ~~said the~~ stress-balancing layer.

18. (Currently Amended) The semiconductor die of claim 17, wherein ~~said the~~ adhesive layer comprises a layer of material for laser-marking.

19. (Currently Amended) A reduced stress semiconductor die, comprising:  
a semiconductor substrate having a front side, a back side, and a low ratio of the height of the semiconductor substrate to a horizontal dimension of the semiconductor substrate;  
an integrated circuit on ~~said~~ the front side of the semiconductor substrate;  
a passivation layer covering a portion of ~~said~~ the integrated circuit causing a force acting on a portion of ~~said~~ the front side; and  
a force-balancing layer covering at least a portion of ~~said~~ the back side, ~~said~~ the force-balancing layer for balancing a portion of ~~said~~ the force on ~~said~~ the front side.

20. (Currently Amended) The semiconductor die of claim 19, wherein ~~said~~ the force-balancing layer comprises one of a single component layer, a substantially homogeneous mixture of a strong material in a matrix material, a heterogeneous composite of particles of a strong material in a matrix material, and a tape with rigidity in the X-Y plane.

21. (Currently Amended) The semiconductor die of claim 19, wherein ~~said~~ the stress-balancing layer comprises an adhesive material.

22. (Currently Amended) The semiconductor die of claim 21, wherein ~~said~~ the stress-balancing layer comprises a layer of material for laser-marking.

23. (Currently Amended) The semiconductor die of claim 19, further comprising an adhesive layer attached to ~~said~~ the stress-balancing layer.

24. (Currently Amended) The semiconductor die of claim 23, wherein ~~said~~ the adhesive layer ~~for laser-marking~~ comprises a layer of material for laser-marking.